CMOS 16-BIT SINGLE-CHIP MICROCOMPUTER

TMP97C241

1. OUTLINE AND CHARACTERISTICS

The TMP97C241 is a high-speed, high-function 16-bit single-chip microcomputer built around a CPU core based on architecture developed by Toshiba. It features built-in bank RAM and other peripheral functions.

TMP97C241 characteristics are as follows:

(1) Original 16-bit CPU
- High-speed, high-function instructions
- 16M-byte linear address space
- General-purpose registers and register bank system

(2) Minimum instruction execution time : 50ns @20MHz

(3) Internal bank RAM : 2K bytes

(4) 10-bit A/D converter : 8 channels

(5) Serial interface : 2 channels
(UART + I/O) and 1 channel (UART)

(6) 16-bit timer : 2 channels

(7) 8-bit timer : 8 channels

(8) Watchdog timer

(9) memory controller : 4 blocks

(10) Interrupt controller:
- 4 CPU interrupts : software interrupt, single-step interrupt, undefined instruction, and illegal operand specification
- 21 internal interrupts :
  20 internal I/Os and 1 task independent delay
- 9 external interrupts :
  8 maskable interrupts and 1 non-maskable interrupt

15-level priority can be set.

(11) Standby functions:
4 software modes : RUN, IDLE1, IDLE2, and STOP
1 hardware mode (PS) : STOP

(12) I/O ports : 96 pins

(13) Package : 120-pin quad flat pack

Type	ROM (byte)	RAM (byte)
* TMP97PS40	64KPROM	2K
* TMP97CS40	64KMROM	2K

* : Under development

2. BLOCK DIAGRAM

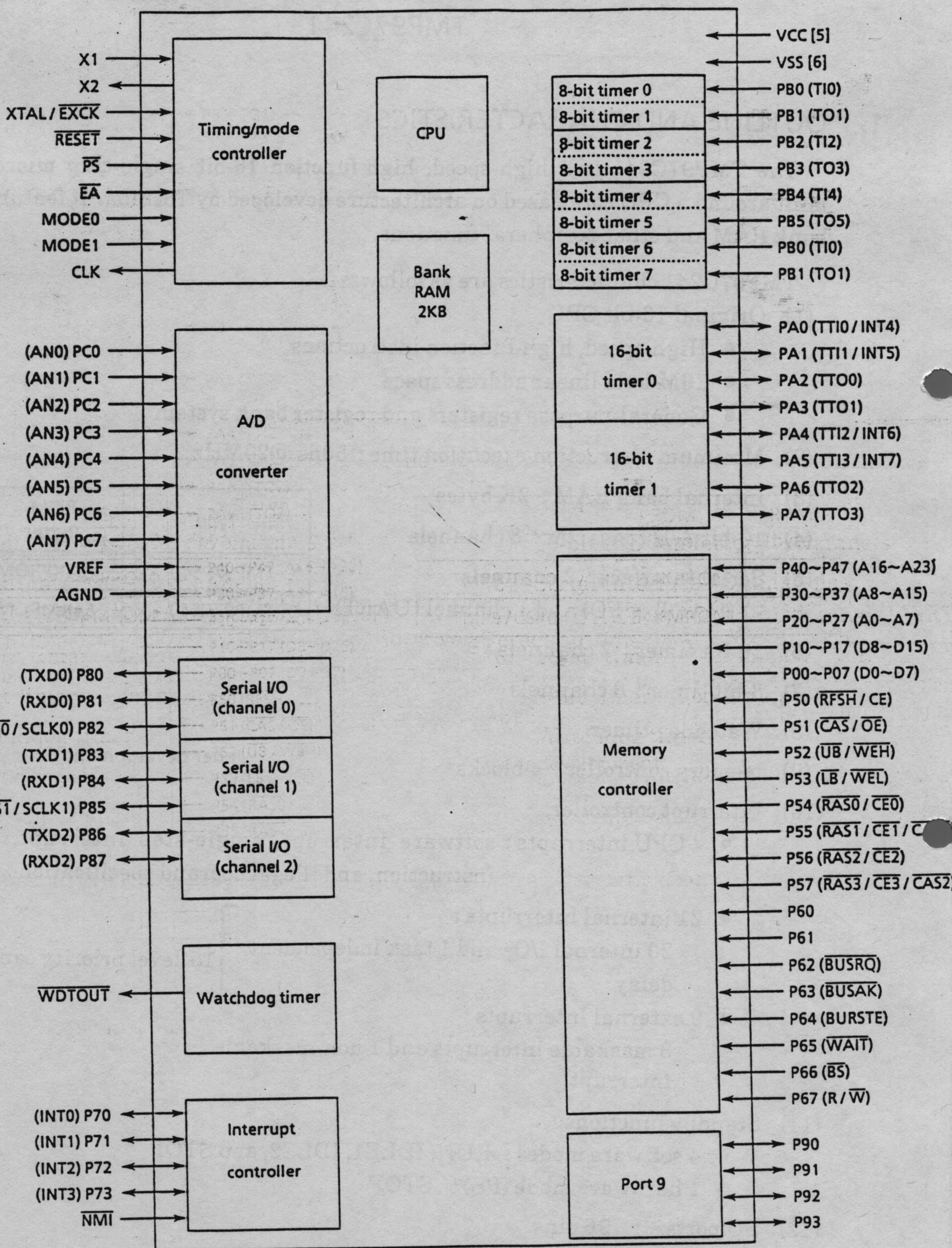
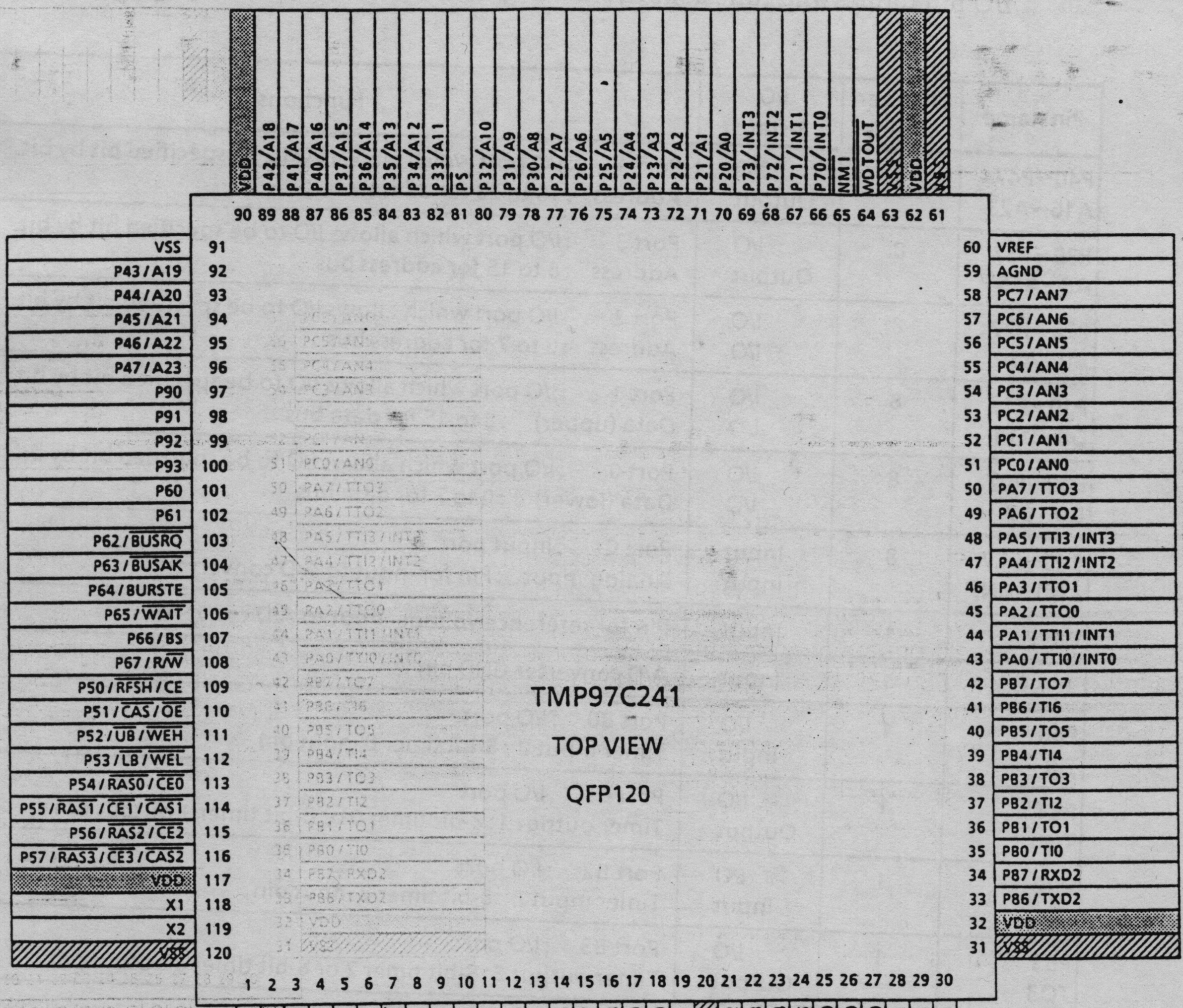


Figure 1 TLCS-9000 Standard MCU block diagram

3. PIN ASSIGNMENT

TLCS-9000 Standard MCU pin assignment



4. PIN NAMES AND FUNCTIONS

I/O pin names and functions are described below:

Pin name	Number of pins	I/O 3-state	Functions
P40~P47 A16~A23	8	I/O Output	Port 4 : I/O port which allows I/O to be specified bit by bit. Address : 16 to 23 for address bus
P30~P37 A8~A15	8	I/O Output	Port 3 : I/O port which allows I/O to be specified bit by bit. Address : 8 to 15 for address bus
P20~P27 A0~A7	8	I/O I/O	Port 2 : I/O port which allows I/O to be specified bit by bit. Address : 0 to 7 for address bus
P10~P17 D8~D15	8	I/O I/O	Port 1 : I/O port which allows I/O to be specified bit by bit. Data (upper) : 8 to 15 for data bus
P00~P07 D0~D7	8	I/O I/O	Port 0 : I/O port which allows I/O to be specified bit by bit. Data (lower) : 0 to 7 for data bus
PC0~PC7 AN0~AN7	8	Input Input	Port C : Input port Analog input : Pin for input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	A/D converter GND pin
PB0 TI0	1	I/O Input	Port B0 : I/O port Timer input 0 : 8-bit timer 0 input pin
PB1 TO0	1	I/O Output	Port B1 : I/O port Timer output 1 : 8-bit timer 0 or 8-bit timer 1 output pin
PB2 TI2	1	I/O Input	Port B2 : I/O port Timer input 2 : 8-bit timer 2 input pin
PB3 TO3	1	I/O Output	Port B3 : I/O port Timer output 3 : 8-bit timer 2 or 8-bit timer 3 output pin
PB4 TI4	1	I/O Input	Port B4 : I/O port Timer input 4 : 8-bit timer 4 input pin
PB5 TO5	1	I/O Output	Port B5 : I/O port Timer output 5 : 8-bit timer 4 or 8-bit timer 5 output pin
PB6 TI6	1	I/O Input	Port B6 : I/O port Timer input 6 : 8-bit timer 6 input pin
PB7 TO7	1	I/O Output	Port B7 : I/O port Timer output 7 : 8-bit timer 6 or 8-bit timer 7 output pin
PA0 TTI0 INT4	1	I/O Input Input	Port A0 : I/O port Timer input 0 : 16-bit timer 0 count/capture trigger input pin Interrupt request pin 4 : Interrupt request pin with programmable rising/falling edge

Pin name	Number of pins	I/O 3-state	Functions
PA1 TTI1 INT5	1	I/O Input Input	Port A1 : I/O port Timer input 1 : 16-bit timer 0 count/capture trigger input pin Interrupt request pin 5 : Interrupt request pin with programmable rising/falling edge
PA2 TO0	1	I/O Output	Port A2 : I/O port Timer output 0: 16-bit timer 0 output pin
PA3 TO1	1	I/O Output	Port A3 : I/O port Timer output 1: 16-bit timer 0 output pin
PA4 TTI2 INT6	1	I/O Input Input	Port A4 : I/O port Timer input 2 : 16-bit timer 1 count/capture trigger input pin Interrupt request pin 6 : Interrupt request pin with programmable rising/falling edge
PA5 TTI3 INT7	1	I/O Input Input	Port A5 : I/O port Timer input 3 : 16-bit timer 1 count/capture trigger input pin Interrupt request pin 7 : Interrupt request pin with programmable rising/falling edge
PA6 TTO2	1	I/O Output	Port A6 : I/O port Timer output 2: 16-bit timer 1 output pin
PA7 TTO3	1	I/O Output	Port A7 : I/O port Timer output 3: 16-bit timer 1 output pin
P90~P93	4	I/O	Port 9 : I/O port which allows I/O to be specified bit by bit.
P70~P73 INT0~3	4	I/O Input	Port 7 : I/O port which allows I/O to be specified bit by bit. External interrupt request pins 0 - 3 : Interrupt request pins with programmable rising/falling edge
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin : Interrupt request pin with falling edge. Can be operated with rising edge by program.
P80 TXD0	1	I/O Output	Port 80 : I/O port Serial send data 0
P81 RXD0	1	I/O Input	Port 81 : I/O port Serial receive data 0
P82 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 82 : I/O port Serial data send enable 0 (Clear To Send) Serial clock I/O 0
P83 TXD1	1	I/O Output	Port 83 : I/O port Serial send data 1

Pin name	Number of pins	I/O 3-state	Functions
P84 RXD1	1	I/O Input	Port 84 : I/O port Serial receive data 1
P85 $\overline{CTS1}$ SCLK1	1	I/O Input	Port 85 : I/O port Serial data send enable 1 (Clear To Send) Serial clock I/O 1
P86 TXD2	1	I/O Output	Port 86 : I/O port Serial send data 2
P87 RXD2	1	I/O Output	Port 87 : I/O port Serial receive data 2
P50 $\overline{RFSH}$ CE	1	I/O Output Output	Port 50 : I/O port Refresh : Connected to pseudo SRAM $\overline{RFSH}$. Chip enable : Connected to SRAM CE2.
P51 $\overline{CAS}$ $\overline{OE}$	1	I/O Output Output	Port 51 : I/O port Column address strobe : Outputs $\overline{CAS}$ strobe for DRAM. Output enable : Strobe signal used to read external memory.
P52 $\overline{UB}$ $\overline{WEH}$	1	I/O Output Output	Port 52 : I/O port Upper byte enable : Strobe signal used to access upper bytes. Upper write enable : Strobe signal used to write D8 - D15 data.
P53 $\overline{LB}$ $\overline{WEL}$	1	I/O Output Output	Port 53 : I/O port Lower byte enable : Strobe signal used to access lower bytes. Lower write enable : Strobe signal used to write D0-D7 data.
P54 $\overline{RAS0}$ $\overline{CE0}$	1	I/O Output Output	Port 54 : I/O port Low address strobe 0 : Outputs $\overline{RAS}$ strobe for DRAM. Chip enable 0 : Outputs 0 when address is within specified address area.
P55 $\overline{RAS1}$ $\overline{CE1}$ $\overline{CAS1}$	1	I/O Output Output Output	Port 55 : I/O port Low address strobe 1 : Outputs $\overline{RAS}$ strobe for DRAM. Chip enable 1 : Outputs 0 when address is within specified address area. Column address strobe 1 : Outputs $\overline{CAS}$ strobe for DRAM when interleave is in use.

Pin name	Number of pins	I/O 3-state	Functions
P56 $\overline{RAS2}$ $\overline{CE2}$	1	I/O Output Output	Port 56 : I/O port Low address strobe 2 : Outputs $\overline{RAS}$ strobe for DRAM. Chip enable 2 : Outputs 0 when address is within specified address area.
P57 $\overline{RAS3}$ $\overline{CE3}$ $\overline{CAS3}$	1	I/O Output Output Output	Port 57 : I/O port Low address strobe 3 : Outputs $\overline{RAS}$ strobe for DRAM. Chip enable 3 : Outputs 0 when address is within specified address area. Column address strobe 2 : Outputs $\overline{CAS}$ strobe for DRAM when interleave is in use.
P64 BURSTE	1	I/O Input	Port 64 : I/O port Burst ready input : Burst fetch enable input. Externally inputs BREADY signal.
P65 $\overline{WAIT}$	1	I/O Input	Port 65 : I/O port READY input : Externally inputs READY signal.
P62 $\overline{BUSRQ}$	1	I/O Input	Port 62 : I/O port Bus request : Signal used to request high impedance for D0-D15, A0-A23, $\overline{CAS}$, $\overline{WEH}$, $\overline{WEL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, CE, $\overline{BS}$, and R/$\overline{W}$ pins. (For external DMAC)
P63 $\overline{BUSAK}$	1	I/O Input	Port 63 : I/O port Bus acknowledge : Signal used to indicate in response to BUSRQ that D0-D15, A0-A23, $\overline{CAS}$, $\overline{WEH}$, $\overline{WEL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, CE, $\overline{BS}$, and R/$\overline{W}$ pins are at high impedance. (For external DMAC)
P66 $\overline{BS}$	1	I/O Output	Port 66 : I/O port Bus start : Signal used to indicate that a valid address is output to address bus.
P67 R/$\overline{W}$	1	I/O Output	Port 67 : I/O port Read/write : Indicates read cycle when set to 1; write cycle, when set to 0.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
CLK	1	Output	Clock output: Outputs x 1/2 clock.
X1 / X2	2	I/O	Oscillator connecting pin
$\overline{RESET}$	1	Input	Reset : Initializes LSI. (With pull-up resistor)
P60	1	I/O	Port 60 : I/O port
P61	1	I/O	Port 61 : I/O port

Pin name	Number of pins	I/O 3-state	Functions
$\overline{EA}$	1	Input	External access : 0 : Should be inputted with TMP97C241 1 : with TMP97C S 40 / TMP97PS40.
MODE (1:0)	2	Input	Mode 1, 0 : Mode switchover signal 00 ..... Normal
$\overline{PS}$	1	Input	Power save input : Inputting 0 to $\overline{PS}$ forcibly halts CPU.
XTAL / $\overline{EXCK}$	1	Input	Oscillator connecting mode when set to 1; external clock input mode, when set to 0.
VCC	5	Input	Power supply pin (+ 5V)
VSS	6	Input	GND pin (0V)

5. MEMORY MAP

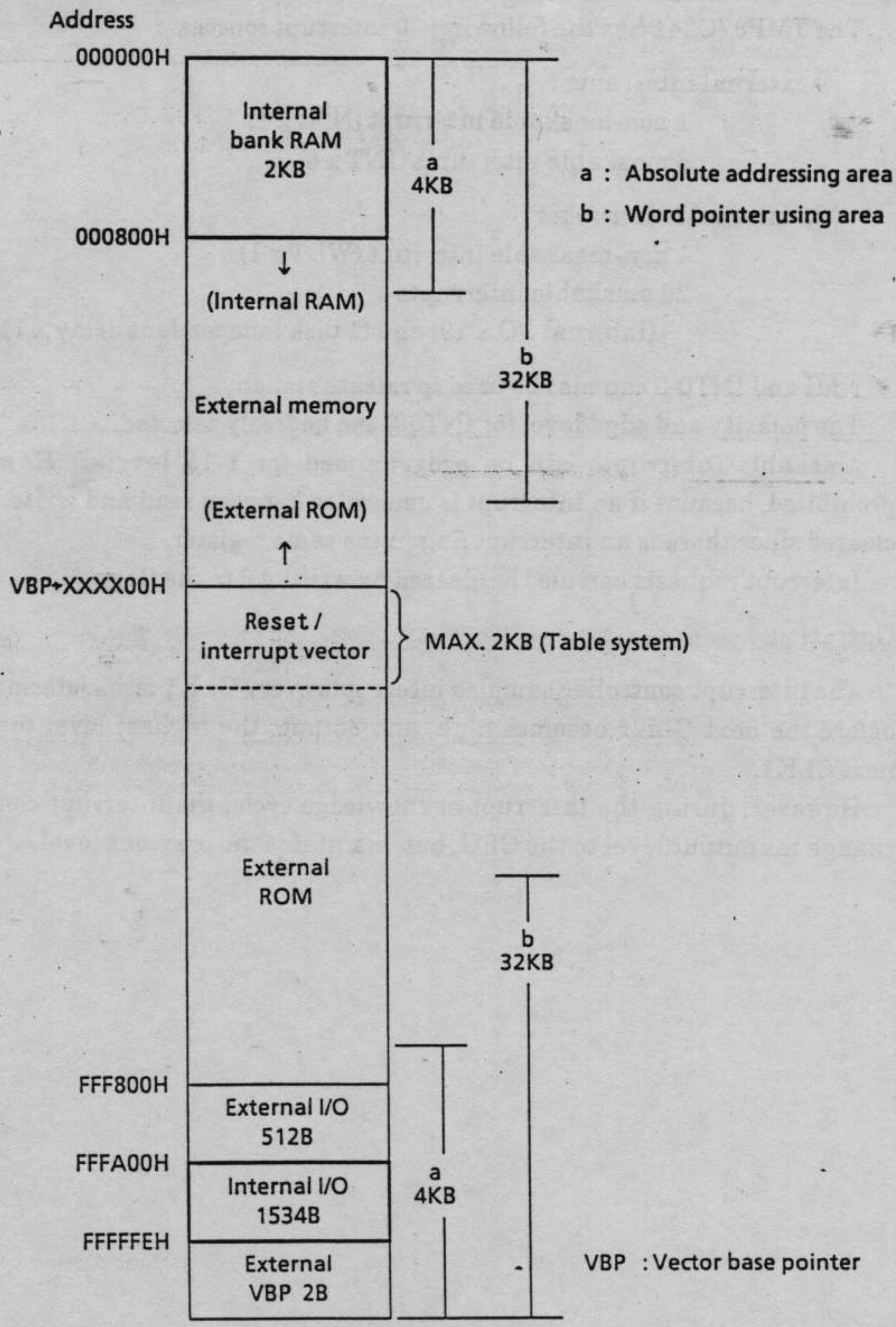


Figure 2 TLCS-9000 Standard MCU memory map

6. INTERRUPT CONTROLLER

The TMP97C241 has the following 30 interrupt sources:

9 external interrupts :

1 non-maskable interrupt ($\overline{NMI}$ x 1)

8 maskable interrupts (INT x 8)

21 internal interrupts :

1 non-maskable interrupt (WDT x 1)

20 maskable interrupts

(internal I/O x 19) and (1 task independent delay x 1)

$\overline{NMI}$ and INT0-3 can also be used to release standby.

The polarity and edge/level for INT0-3 can be freely selected.

Maskable interrupts can be programmed for 1-15 levels. However, RMW is prohibited, because if an interrupt is generated between read and write, the interrupt is cleared since there is an interrupt flag in the same register.

Interrupt requests can also be cleared by writing 0 to the flag.

Operation:

The interrupt controller samples interrupts every CLK1 rise, determines the priority before the next CLK1 becomes high, and outputs the highest level to the CPU at the next CLK1.

However, during the interrupt acknowledge cycle, the interrupt controller does not change the output level to the CPU, but maintains the previous level.

Interrupt Table

Symbol	Type	Internal / external	Default priority	Interrupt request generation source	Vector number
NMI	Non-maskable	External	1	$\overline{\text{NMI}}$ pin	
INTWD		Internal	1	Watchdog timer	
INT0	Maskable	External	1	INT0 pin	20H
INT1			2	INT1 pin	21H
INT2			3	INT2 pin	22H
INT3			4	INT3 pin	23H
INT4			5	INT4 pin	24H
INT5			6	INT5 pin	25H
INT6			7	INT6 pin	26H
INT7			8	INT7 pin	27H
INTT0		Internal	9	8-bit Timer 0	28H
INTT1			10	8-bit Timer 1	29H
INTT2			11	8-bit Timer 2	2AH
INTT3			12	8-bit Timer 3	2BH
INTT4			13	8-bit Timer 4	2CH
INTT5			14	8-bit Timer 5	2DH
INTT6			15	8-bit Timer 6	2EH
INTT7			16	8-bit Timer 7	2FH
INTTR0			17	16-bit Timer 0	30H
INTTR1			18	16-bit Timer 0	31H
INTTR2			19	16-bit Timer 1	32H
INTTR3			20	16-bit Timer 1	33H
INTRX0			21	Serial receive 0	34H
INTTX0			22	Serial send 0	35H
INTRX1			23	Serial receive 1	36H
INTTX1			24	Serial send 1	37H
INTRX2			25	Serial receive 2	38H
INTTX2			26	Serial send 2	39H
INTAD			27	A/D conversion	3AH
INTTASK			28	Task independent delay	03H
				Erroneous interrupt	04H

7. STANDBY FUNCTIONS

When the halt instruction is executed, the TMP97C241 enters RUN, IDLE1, IDLE2, or STOP mode depending on the contents of the halt mode setting register.

(1) RUN mode : Only the CPU halts; power consumption remains unchanged.

(2) IDLE1 mode : Only the built-in oscillator operates; other circuits halt. Power consumption is reduced to 1/10 or less than that during normal operation.

(3) IDLE2 mode : The built-in oscillator and some specific internal I/Os operates. Power consumption is reduced to 1/3 or less than that during normal operation.

(4) STOP mode : All internal circuits including the built-in oscillator halt. Power consumption is greatly reduced.

The states of the port pins in STOP mode can be set as listed in Table ?? using the WDMOD<DRVE> bit in the I/O register.

WDMOD	7	6	5	4	3	2	1	0
bit symbol	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE
Read / Write	R/W							
After reset	1	0	0	0	0	0	0	0
Function	1 : WDT Enable	00 : 2^{18}/fc 01 : 2^{20}/fc 10 : 2^{22}/fc 11 : 2^{24}/fc	Detection time	Warming up time 0 : 2^{16}/fc 1 : 2^{18}/fc	Standby mode 00 : RUN mode 01 : STOP mode 10 : IDLE1 mode 11 : IDLE2 mode		1 : Internally connects watchdog timer output to $\overline{\text{RESET}}$ pin.	1 : Drives pin even in STOP mode.

When STOP mode is released by other than a reset, the system clock output starts after allowing some warm-up time (set by the warming-up counter for stabilizing the built-in oscillator). To release STOP mode by a reset, it is necessary to allow a reset time long enough for the oscillator to stabilize.

To release standby mode, a reset or an interrupt is used. To release IDLE1 or STOP mode, only an interrupt by the $\overline{\text{NMI}}$ or INT0-3 pin, or a reset can be used. The details are described below.

Standby release by interrupts

Interrupt level / Halt mode	Interrupt mask (IM0-IM3) < Interrupt request level	Interrupt mask (IM0-IM3) ≥ Interrupt request level
RUN	Can be released by any interrupt. After standby release, interrupt processing starts.	Cannot be released. (No change)
IDLE2	Can be released by interrupts other than A/D conversion end interrupt (INTAD). After standby release, interrupt processing starts. (Clock is supplied to the interrupt controller.)	RUN mode is automatically entered by an interrupt other than A/D conversion end interrupt (INTAD) and an interrupt at a higher level is awaited. (Clock is supplied to the interrupt controller.)
IDLE1	Can only be released by $\overline{\text{NMI}}$ or INT0-INT3 pin. After standby release, interrupt processing starts. (Clock is supplied to the interrupt controller.)	RUN mode is automatically entered by a $\overline{\text{NMI}}$ or the INT0-INT3 pin and an interrupt at a higher level is awaited. (Clock is supplied to the interrupt controller.)
STOP	Can only be released by $\overline{\text{NMI}}$ or INT0-INT3 pin. After standby release, interrupt processing starts. (After the built-in oscillator starts operation, clock is supplied to the interrupt controller.)	RUN mode is automatically entered by a $\overline{\text{NMI}}$ or the INT0-INT3 pin and an interrupt at a higher level is awaited. (After the built-in oscillator starts operation, clock is supplied to the interrupt controller.)

Pin states in STOP mode

Pin name	I/O	DRVE = 0	DRVE = 1
P0, P1	Input mode/ D0~D7, D8~D15 Output mode	—* —*	— Output
P2, P3, P4	Input mode Output mode/ A0~A7, A8~A15, A16~A23	—* —*	Input Output
P50	Input mode Output mode	PD* PD*	PD Output
P51~P57, P6	Input mode Output mode	PU* PU*	PU Output
P7	Input mode/ INT0~INT3 Output mode	—/Input —	—/Input Output
P80, P83, P86	Input mode Output mode	PU* PU*	PU Output
P81, P82, P84, P85, P87	Input mode Output mode	PU* PU*	PU Output
P9	Input mode Output mode	PU* PU*	PU Output
PA	Input mode Output mode	PU* PU*	PU Output
PB	Input mode Output mode	PU* PU*	PU Output
PC	Input mode Output mode	PU* PU*	PU Output
$\overline{\text{RESET}}$	Input	Input	Input
X1	Input	—	—
X2	Output	"0"	"0"
XTAL/ $\overline{\text{EXCK}}$	Input	Input	Input
$\overline{\text{EA}}$	Input	Input	Input
CLK	Output	"1"	"1"
MODE0, MODE1	Input	Input	Input
$\overline{\text{PS}}$	Input	Input	Input
$\overline{\text{WDTOUT}}$	Output	Output	Output
$\overline{\text{NMI}}$	Input	Input	Input

— : Input for input mode/input pin is invalid; output mode/output pin is at high impedance.

Input : Input enabled.

Input : Input gate in operation. Fix the input voltage to 0 or 1 so that the input pin stays still.

Output : Output state

PU : Pin with a programmable pull-up resistor. Fix the pin to avoid through current since the input gate is in operation when a pull-up resistor is not set.

PD : Pin with a programmable pull-down resistor. Fix the pin to avoid through current since the input gate is in operation when a pull-down resistor is not set.

* : Input gate disabled. No through current since the output buffer is disconnected.

I/O operations during halt and halt release sources

Halt mode			RUN	IDLE2	IDLE1	STOP
WDMOD<HALTM1.0>			00	11	10	01
Operation block	CPU		Halt*	Halt		
	I/O port		Maintains states when the halt instruction is executed.			*1
	8-bit timer		Operation	Halt		
	16-bit timer					
	Serial interface					
	A/D converter					
	Watchdog timer					
	Memory controller					
	Interrupt controller					
Halt release source	Interrupt	NMI	○	○	○	○
		INT0~3	○	○	○	○
		INTT0	○	○	—	—
		INTT1	○	○	—	—
		INTT2	○	○	—	—
		INTT3	○	○	—	—
		INTT4	○	○	—	—
		INTT5	○	○	—	—
		INTT6	○	○	—	—
		INTT7	○	○	—	—
		INT4	○	○	—	—
		INT5	○	○	—	—
		INTTR4	○	○	—	—
		INTTR5	○	○	—	—
		INT6	○	○	—	—
		INT7	○	○	—	—
		INTTR6	○	○	—	—
		INTTR7	○	○	—	—
		INTTX0	○	○	—	—
		INTRX0	○	○	—	—
		INTTX1	○	○	—	—
		INTRX1	○	○	—	—
		INTTX2	○	○	—	—
		INTRX2	○	○	—	—
		INTAD	○	—	—	—
		INTWD	○	○	—	—
	Reset		○	○	○	○

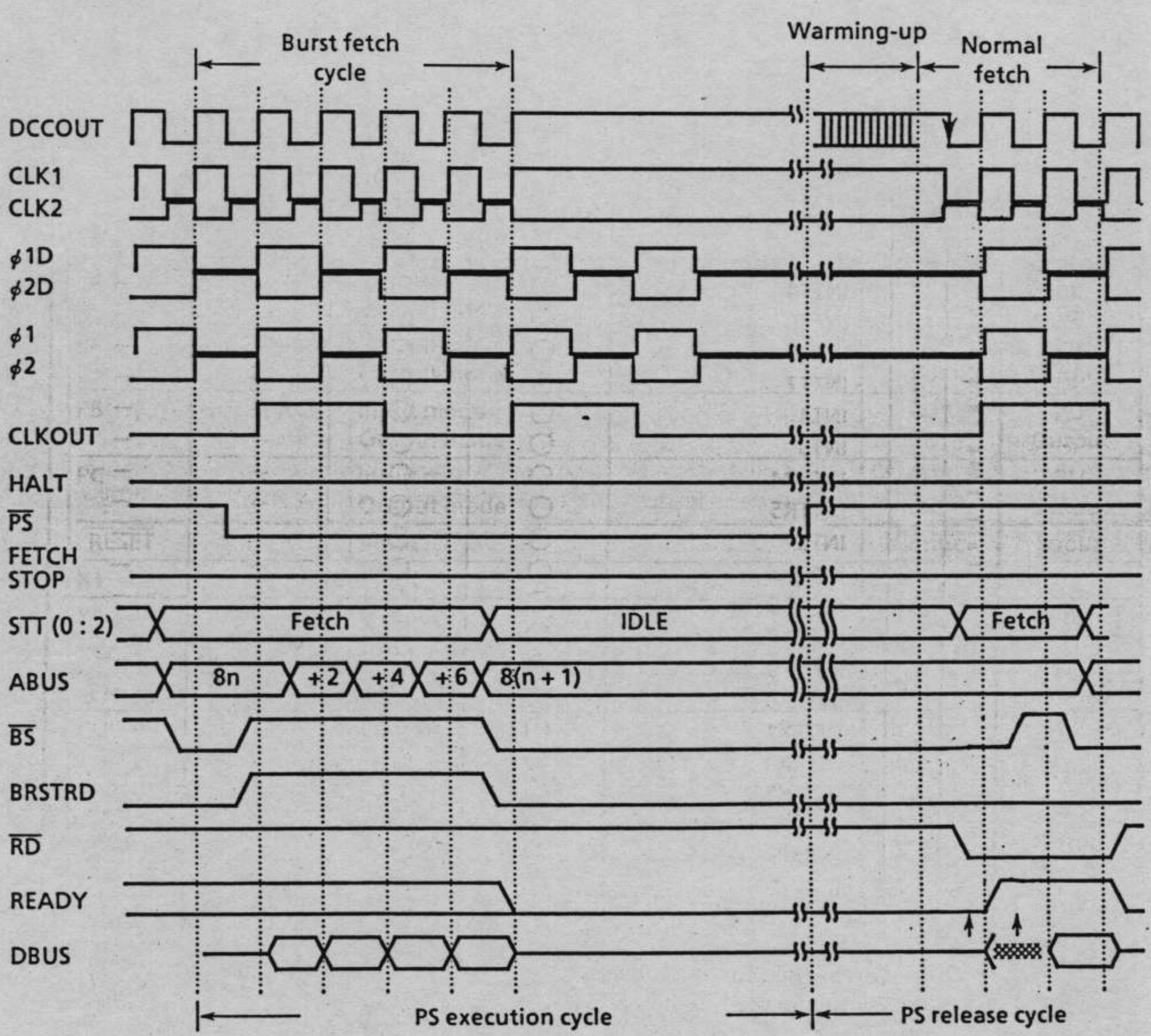
○ : Can be used for halt release.
— : Cannot be used for halt release.

* : Clock is operating and a NOP is executed.
*1 : See Table on Pin states in STOP mode on the previous page.

Power save (Hardware standby)

Setting the $\overline{PS}$ signal to 0 halts all the internal circuits including the built-in oscillator. In this mode, internal power consumption is greatly reduced. Setting the $\overline{PS}$ signal to 1 releases this mode. At release, the system clock output starts after the warming-up time set by the warm-up counter.

Power save sets each pin to the same state as that in STOP mode by the halt instruction.



Hardware standby timing chart

8. PORT FUNCTIONS

The TMP97C241 has a total of 96 bits for I/O ports.

These port pins are used for I/Os for the internal CPU and internal I/Os as well as general-purpose I/O ports.

(R : ↑ = With programmable pull-up resistor.
↓ = With programmable pull-down resistor.)

Port name	Pin name	Number of pins	Direction	R	Direction setting unit	State after reset		Name of pin for internal function
						$\overline{EA}$ = 1	$\overline{EA}$ = 0	
Port 0	P00~P07	8	I/O	—	Bit	Port input	D0~D7 (I/O)	D0~D7
Port 1	P10~P17	8	I/O	—	Bit	Port input	D8~D15 (I/O)	D8~D15
Port 2	P20~P27	8	I/O	—	Bit	Port input	A0~A7 (Output)	A0~A7
Port 3	P30~P37	8	I/O	—	Bit	Port input	A8~A15 (Output)	A8~A15
Port 4	P40~P47	8	I/O	—	Bit	Port input	A16~A23 (Output)	A16~A23
Port 5	P50	1	I/O	↓	Bit	Port input	Port input	$\overline{RFSH}$/$\overline{OE}$/CE
	P51	1	I/O	↑	Bit	Port input	$\overline{OE}$ (Output)	$\overline{CAS}$/$\overline{OE}$
	P52	1	I/O	↑	Bit	Port input	$\overline{WEH}$ (Output)	$\overline{WEH}$/$\overline{UB}$
	P53	1	I/O	↑	Bit	Port input	$\overline{WEL}$ (Output)	$\overline{WEL}$/$\overline{LB}$
	P54	1	I/O	↑	Bit	Port input	Port input	$\overline{RAS0}$/$\overline{CE0}$
	P55	1	I/O	↑	Bit	Port input	Port input	$\overline{RAS1}$/$\overline{CE1}$/$\overline{CAS1}$
	P56	1	I/O	↑	Bit	Port input	Port input	$\overline{RAS2}$/$\overline{CE2}$
	P57	1	I/O	↑	Bit	Port input	$\overline{CE3}$ (Output)	$\overline{RAS3}$/$\overline{CE3}$/$\overline{CAS2}$
Port 6	P60	1	I/O	↑	Bit	Port input	Port input	
	P61	1	I/O	↑	Bit	Port input	Port input	
	P62	1	I/O	↑	Bit	Port input	Port input	$\overline{BUSRQ}$
	P63	1	I/O	↑	Bit	Port input	Port input	$\overline{BUSAK}$
	P64	1	I/O	↑	Bit	Port input	BURSTE (Input)	BURSTE
	P65	1	I/O	↑	Bit	Port input	$\overline{WAIT}$ (Input)	$\overline{WAIT}$
	P66	1	I/O	↑	Bit	Port input	$\overline{BS}$ (Output)	$\overline{BS}$
	P67	1	I/O	↑	Bit	Port input	R/$\overline{W}$ (Output)	R/$\overline{W}$
Port 7	P70~P73	4	I/O	—	Bit	Port input	Port input	INT0~INT3
Port 8	P80	1	I/O	↑	Bit	Port input	Port input	TXD0
	P81	1	I/O	—	Bit	Port input	Port input	RXD0
	P82	1	I/O	—	Bit	Port input	Port input	$\overline{CTS0}$/SCLK0
	P83	1	I/O	↑	Bit	Port input	Port input	TXD1
	P84	1	I/O	—	Bit	Port input	Port input	RXD1
	P85	1	I/O	—	Bit	Port input	Port input	$\overline{CTS1}$/SCLK1
	P86	1	I/O	↑	Bit	Port input	Port input	TXD2
	P87	1	I/O	—	Bit	Port input	Port input	RXD2
Port 9	P90~P93	4	I/O	—	Bit	Port input	Port input	
Port A	PA0	1	I/O	—	Bit	Port input	Port input	TTI0/INT4
	PA1	1	I/O	—	Bit	Port input	Port input	TTI1/INT5
	PA2	1	I/O	—	Bit	Port input	Port input	TTO0
	PA3	1	I/O	—	Bit	Port input	Port input	TTO1
	PA4	1	I/O	—	Bit	Port input	Port input	TTI2/INT6
	PA5	1	I/O	—	Bit	Port input	Port input	TTI3/INT7
	PA6	1	I/O	—	Bit	Port input	Port input	TTO2
	PA7	1	I/O	—	Bit	Port input	Port input	TTO3
Port B	PB0	1	I/O	—	Bit	Port input	Port input	TI0
	PB1	1	I/O	—	Bit	Port input	Port input	TO1
	PB2	1	I/O	—	Bit	Port input	Port input	TI2
	PB3	1	I/O	—	Bit	Port input	Port input	TO3
	PB4	1	I/O	—	Bit	Port input	Port input	TI4
	PB5	1	I/O	—	Bit	Port input	Port input	TO5
	PB6	1	I/O	—	Bit	Port input	Port input	TI6
	PB7	1	I/O0	—	Bit	Port input	Port input	TO7
Port C	PC0~PC7	8	Input	—	(Fixed)	Port input	Port input	AN0~AN7

Resetting makes these port pins general-purpose I/O ports.

I/O pins programmable for input or output function as input ports.

Programmable pull-up or pull-down resistors are in connected state.

When port pins are used for internal functions, they must be set by program.

Setting bus request signal $\overline{BUSRQ}$ to 0 sets the following pins to high impedance. The internal programmable pull-up or pull-down resistors continue to function.

Pin name	Condition for high impedance
D0~D7 D8~D15 A0~A7 A8~A15 A16~A23 $\overline{RFSH}/\overline{OE}$/CE $\overline{CAS}/\overline{OE}$ $\overline{WEH}/\overline{UB}$ $\overline{WEL}/\overline{LB}$ $\overline{RAS0}/\overline{CE0}$ $\overline{RAS1}/\overline{CE1}/\overline{CAS1}$ $\overline{RAS2}/\overline{CE2}$ $\overline{RAS3}/\overline{CE3}/\overline{CAS2}$ $\overline{BUSRQ}$ $\overline{BUSAK}$ BURSTE $\overline{WAIT}$ $\overline{BS}$ R/$\overline{W}$	$\overline{BUSRQ}$ = 0 and not set as I/O port pin.

Internal memory or internal I/O of the TMP97C241 cannot be accessed with an external DMA controller.

9. PORT 9

Port 9 is a 4-bit general-purpose I/O port which allows I/Os to be specified bit by bit. I/Os are specified using control register P9CR. Resetting sets all bits in output latch P9 and all bits in control register P9CR to 0 and port 9 is set to an input port.

10. MEMORY CONTROLLER

1. Outline

The Memory Controller Unit (MECU) controls DRAM, SRAM, pseudo SRAM, and I/Os.

The MECU automatically generates all the signals necessary for interface eliminating the need for external components.

The MECU can independently control four types of memory using the $\overline{RAS}/\overline{CE}$ of the four channels.

2. Signal line description

Signal name	Function
CLK1	System clock 1
CLK2	System clock 2
$\overline{RAS0}/\overline{CE0}$	Connected to $\overline{RAS}$ in DRAM mode and $\overline{CE}$ in SRAM mode.
$\overline{RAS1}/\overline{CE1}/\overline{CAS1}$	Connected to $\overline{RAS}$ in DRAM mode and $\overline{CE}$ in SRAM mode. Connected to $\overline{CAS}$ when using interleave.
$\overline{RAS2}/\overline{CE2}$	onnected to $\overline{RAS}$ in DRAM mode and $\overline{CE}$ in SRAM mode.
$\overline{RAS3}/\overline{CE3}/\overline{CAS2}$	Connected to $\overline{RAS}$ in DRAM mode and $\overline{CE}$ in SRAM mode. Connected to $\overline{CAS}$ when using interleave.
$\overline{CAS}/\overline{OE}$	Connected to $\overline{CAS}$ in DRAM mode and $\overline{OE}$ in SRAM mode.
R/$\overline{W}$	Indicates CPU operating state.
$\overline{UB}$	Strobe signal at upper byte access
$\overline{LB}$	Strobe signal at lower byte access
$\overline{RFSH}$/CE	Connected to CE2 of SRAM and $\overline{RFSH}$ of pseudo SRAM. Backs up memory in standby mode.
BURSTE	Burst fetch enable input. Externally inputs BREADY signal.
$\overline{WAIT}$	READY signal input. Externally inputs READY signal. BURSTE/$\overline{WAIT}$ signals become valid after waits are automatically and internally inserted.
A (23 : 0)	Address bus
D (15 : 0)	Data bus

3. Control registers

3.1 CHREG0-3: Used to set $\overline{RAS}/\overline{CE}$ signal output range, memory type, and wait time for the channels.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHREGn (n = 0-3) FFFFF0 ~FFFFF7	can23	can22	can21	can20	can19	can18	can17	b16n	wpn	memn1	memn0	sizen2	sizen1	sizen0	chmodn1	chmodn0

can (23:17) Compares the value in can register (A (9:3) for IO devices; otherwise, A (23:17)) with the upper address accessed by the CPU . If matched, outputs $\overline{RAS}/\overline{CE}$ signal. The range for comparison is determined by sizen (2:0).

b16n Controls $\overline{UB}$ and $\overline{LB}$ signals.

0 : Outputs only at write.

1 : Outputs at both write and read.

16-bit bus memory generally contains a byte control pin which is used for this control.

wpn Disables write.

0 : Enables write.

1 : Disables write.

memn (1:0) Indicates memory type.

00 : IO device sizen (2:0) is other than 111.

01 : Pseudo SRAM

10 : SRAM

11 : DRAM

sizen (2:0) Indicates the range for address comparison.

	ca23	ca22	ca21	ca20	ca19	ca18	ca17	Size (W)
111:	–	–	–	–	–	–	–	8M
110:	*	–	–	–	–	–	–	4M
101:	*	*	–	–	–	–	–	2M
100:	*	*	*	–	–	–	–	1M
011 :	*	*	*	*	–	–	–	512K
010:	*	*	*	*	*	–	–	256K
001:	*	*	*	*	*	*	–	128K
000:	*	*	*	*	*	*	*	64K

– Does not compare

* Compares

Comparison object	a23	a22	a21	a20	a19	a18	a17	Other than IO devices
	a9	a8	a7	a6	a5	a4	a3	IO devices

chmod (1:0) Sets wait time and burst enable.

IO device :	All cycles	Wait	Burst
01 :	2 clock	0 clock	Disabled
10 :	3 clock	1 clock	Disabled
11 :	4 clock	2 clock	Disabled
00 :	5+n clock	3+n clock	Disabled

n : Additional waits can be inserted by externally inputting the $\overline{WAIT}$ signal, as well as the waits specified by program.

SRAM :	All cycles	Wait	Burst
00 :	2 clock	0 clock	Enabled
01 :	2 clock	0 clock	Disabled
10 :	3 clock	1 clock	Disabled
11 :	4+n clock	2+n clock	Disabled

DRAM :	All cycles	Wait	Burst	Precharge	Notes
00 :	3 clock	1 clock	Enabled	1 clock	Interleave
01 :	5+n clock	3+n clock	Enabled	2 clock	Interleave
10 :	3 clock	1 clock	Disabled	1 clock	
11 :	5+n clock	3+n clock	Disabled	2 clock	

Pseudo SRAM :	All cycles	Wait	Burst	Precharge	Notes
00 :	4 clock	2 clock	Disabled	2 clock	
01 :	5 clock	3 clock	Disabled	2 clock	
10 :	6 clock	4 clock	Disabled	3 clock	
11 :	7+n clock	5+n clock	Disabled	3 clock	

When memn (1 : 0) is 00 and sizen (2 : 0) are all 1s, operation of the corresponding channel is disabled.

3.2 REFHREG: Used to set refresh cycle and all other data for the memory controller.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REFHREG FFFFF8	cycle1	cycle2	refhall	start	psoen	pageen	defen	defb16	defwp	defmem1	defmem0	"0"	"0"	"0"	defch1	defch0

cycle (1:0) Indicates refresh cycle.

refhall Sets whether all channels are refreshed simultaneously or individually.

cycle (1:0) :	refhall=0	refhall=1
00 :	Every 16 clocks	Every 64 clocks
01 :	Every 32 clocks	Every 128 clocks
10 :	Every 64 clocks	Every 256 clocks
11 :	Every 128 clocks	Every 512 clocks

Note 1 : When refhall = 1, refresh output is generated at ch0 timing.
Thus, refresh is performed at 4 x clock when refhall = 0.

Note 2 : Refresh output is performed to the channel set in DRAM pseudo SRAM.
If there is no corresponding channel, refresh is not performed.

start Writing 1 to this bit when ch3 only is valid after a reset validates the settings in chreg (0-3). The settings do not change even if 0s are written afterwards.

psoen Outputs $\overline{OE}$ signals from the $\overline{RFSH}$ pin only if the pseudo SRAM is connected.
Set this bit to 1 when connecting the pseudo SRAM with the $\overline{RFSH/OE}$ pin.

	$\overline{RFSH}$ pin
0 :	$\overline{RFSH}$ output only
1 :	$\overline{RFSH/OE}$ output

pageen Set this bit to 1 when enable the page made access in DRAM.

defen Set this bit to 1 when validates the settings in the default state.

def··· Controls wait time in the default state (when an external memory area other than the address area set in chreg (0-3) is accessed) and output pin states.

defb16 b16 signal in default state

defwp wp signal in default state

defmem (1:0) mem (1:0) signal in default state

defch (1:0) chmod (1:0) signal in default state

In default state, $\overline{RAS/CE}$ signals are not output. However, address and $\overline{BS}$ signals are output as-are so that the external memory controller and the VRAM processor can be connected.

4. Operation after a reset (bootstrap)

There are two modes after a reset: single-chip mode and external bus mode. In either mode, when the area where the internal memory locates is accessed, the internal memory is accessed. The memory controller operates only in the external memory area. The difference between single-chip mode and external bus mode is determined by whether the internal ROM is valid. In external bus mode, the external ROM is used instead of the internal ROM.

After a reset is released, ch3 of the memory controller becomes valid all over the external memory. While ch3 is valid, only the start bit (b13) in REFHREG is set. Thus, the user first sets CHREG0-3, then writes data to REFHREG, and starts the memory controller.

The contents of CHREG (0-3) and REFHREG are held until a reset.

Settings can be done again except for the start bit in REFHREG.

In single-chip mode, I/O pins after a reset are set to I/O. The user program is started by the internal ROM and switches all the necessary I/O pins to the memory controller.

In external bus memory, all pins other than those for signals necessary to operate ch3 memory (usually ROM) are set to I/O. The states of the pins after a reset are as follows:

Used for the memory controller:

$\overline{RAS3}/\overline{CE3}$, $\overline{CAS}/\overline{OE}$, $R/\overline{W}$, $\overline{UB}$, $\overline{LB}$, A (13:0) , BURSTE, $\overline{WAIT}$, D (15:0), $\overline{BS}$

Used for I/O:

$\overline{RAS0}/\overline{CE0}$, $\overline{RAS1}/\overline{CE1}/\overline{CAS1}$, $\overline{RAS2}/\overline{CE2}$, $\overline{RFSH}$/CE, $\overline{BUSRQ}$, $\overline{BUSAK}$

-------→ P5 (6-4, 0) , P6 (3, 2)

Can be set for each product:

A (23:14)

5. Memory controller connecting example

Notes:

(1) DRAM mode address

In DRAM mode, the low and high addresses are multiplexed and output. Connect in alignment with the column addresses.

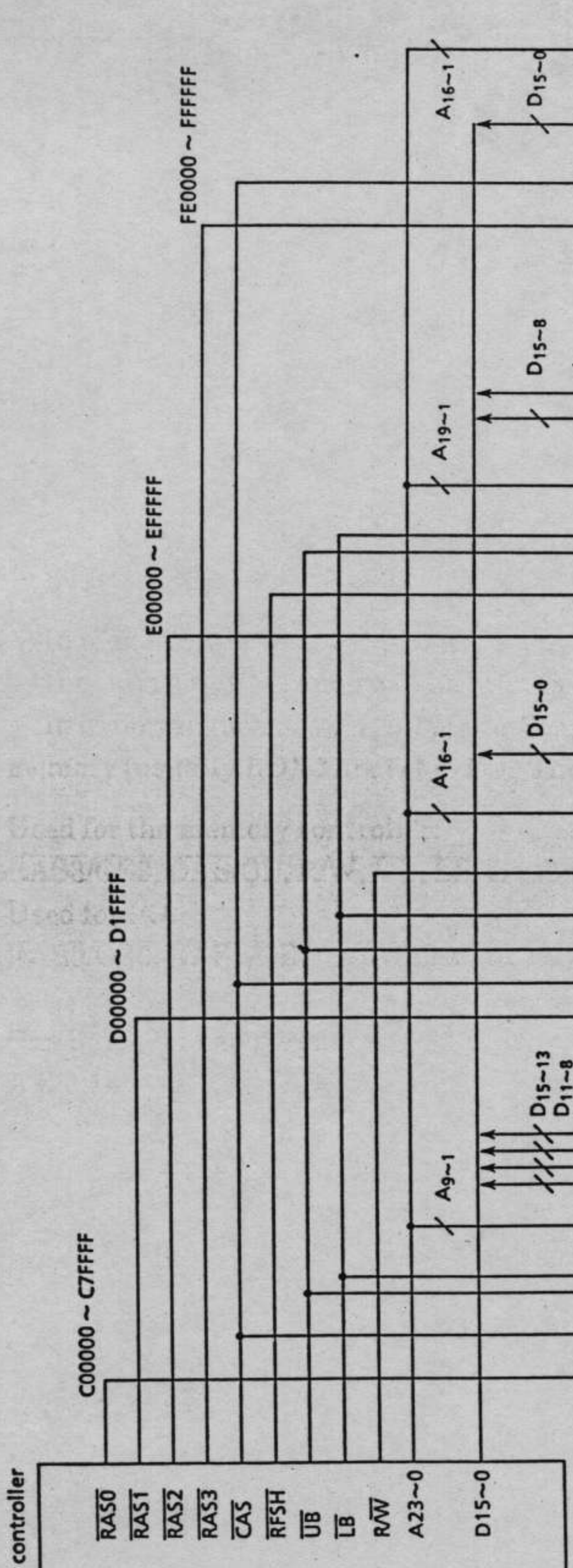
(2) $\overline{UB}$ and $\overline{LB}$ pins

With 16-bit bus SRAM, use these pins for $\overline{UB}$ and $\overline{LB}$ signals by setting the b16n bit in the control register to 1. With other memories, use these pins for $\overline{WEH}$ and $\overline{WEL}$ signals by setting the b16bn bit to 0.

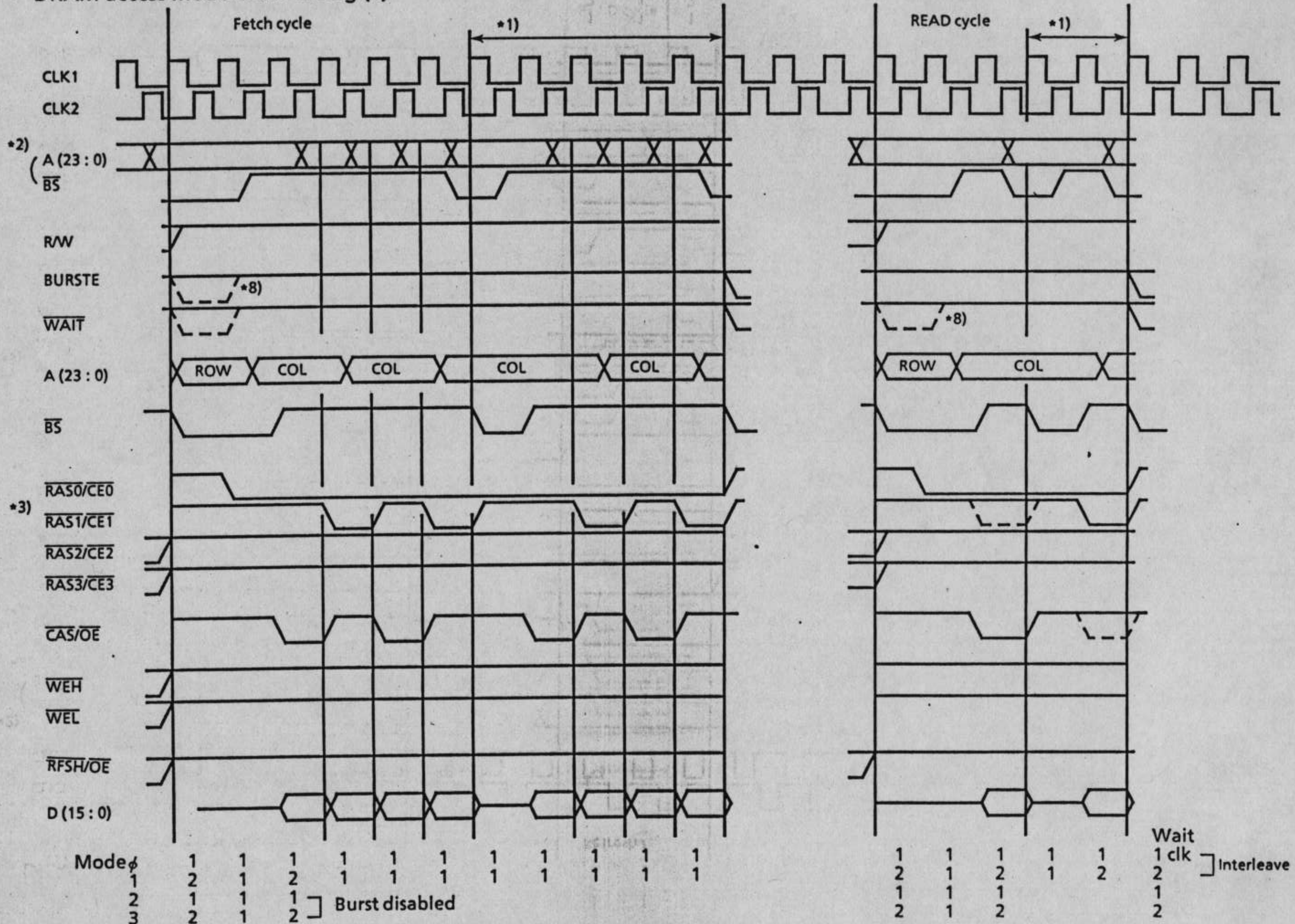
(3) PSRAM refresh

When $\overline{OE}$ and $\overline{RFSH}$ are controlled by the same pin, set the psoen bit in REFHREG to 1.

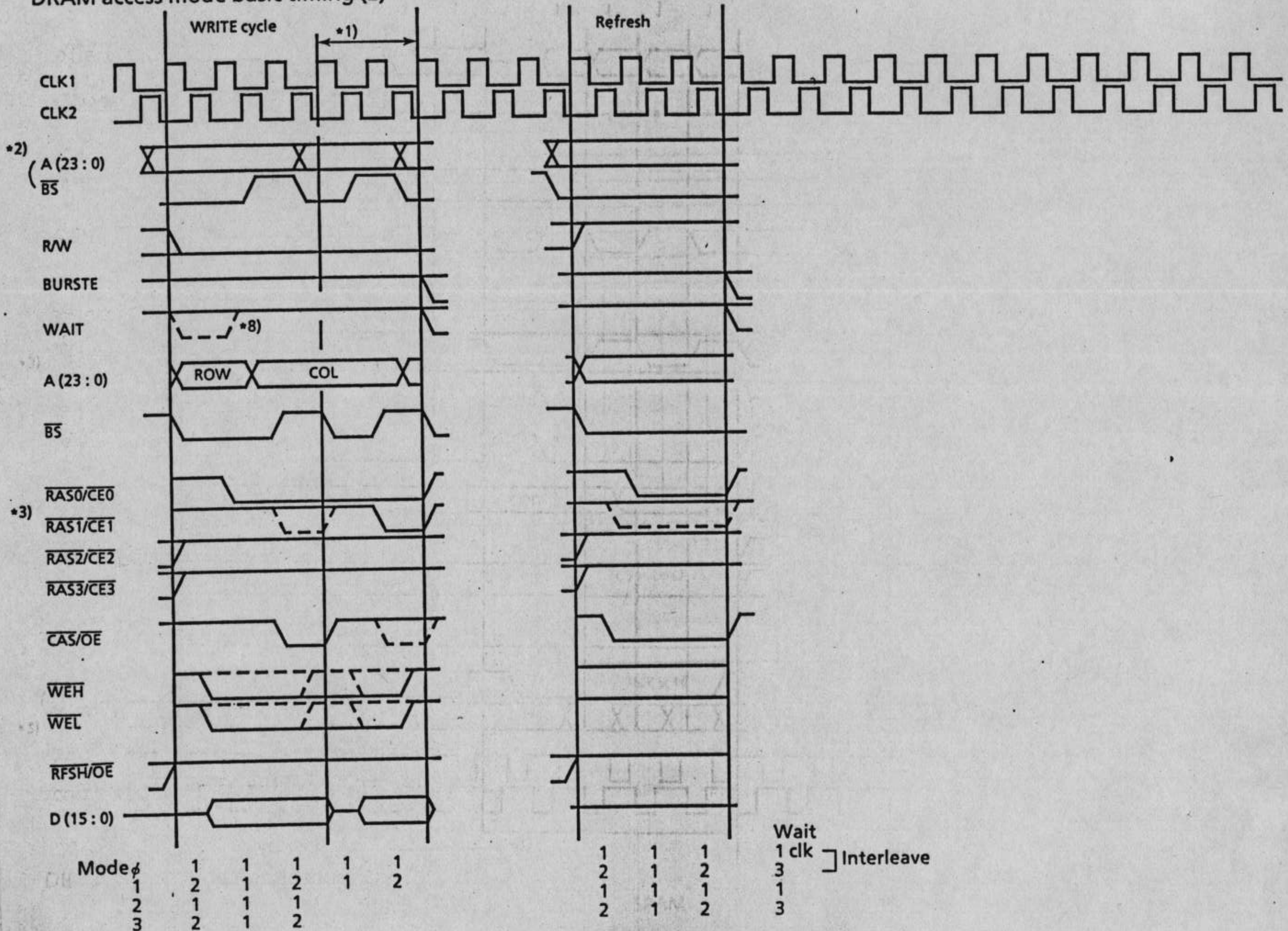
connecting example



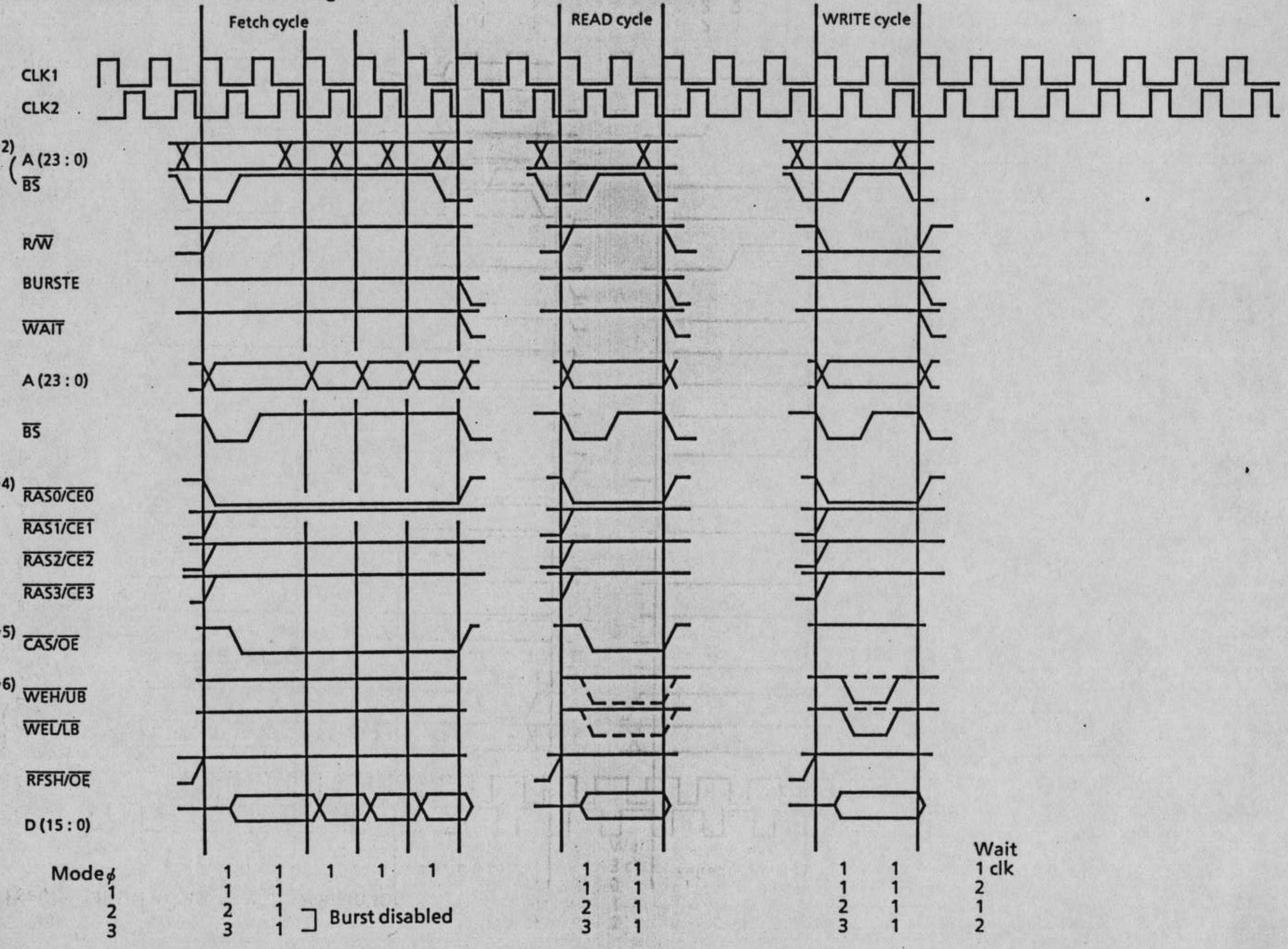
DRAM access mode basic timing (1)



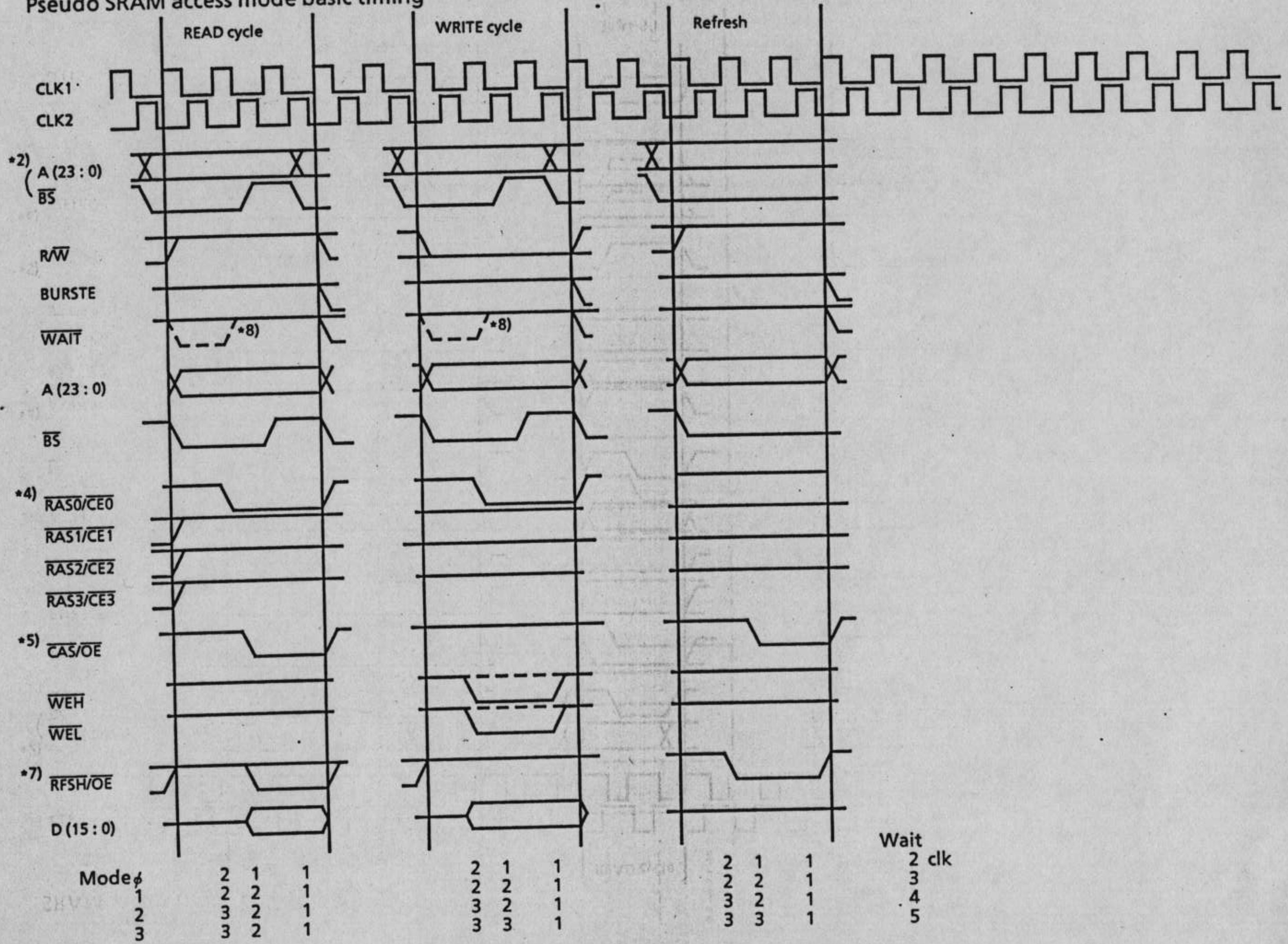
DRAM access mode basic timing (2)



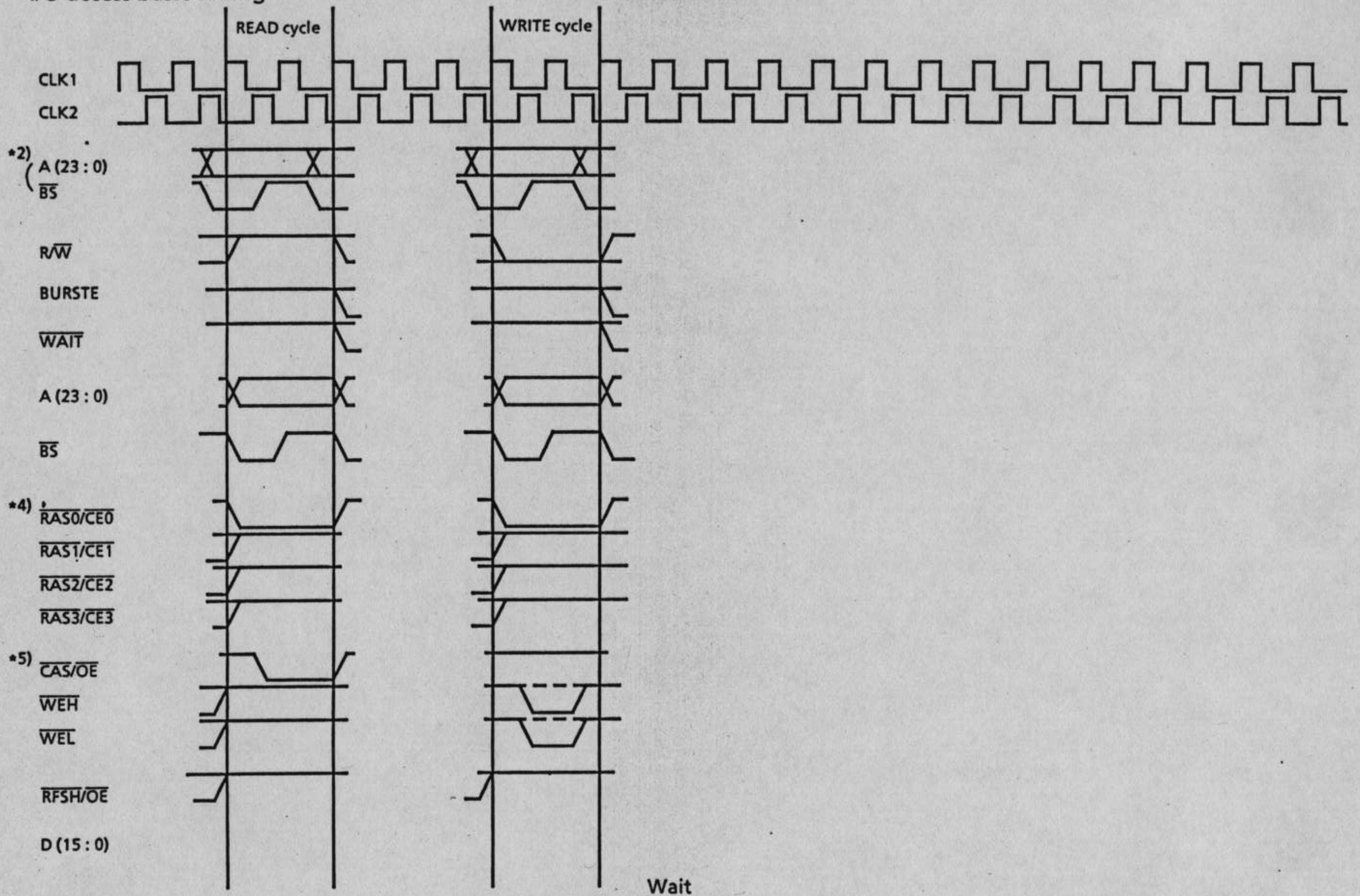
SRAM access mode basic timing



Pseudo SRAM access mode basic timing



I/O access basic timing



Mode	φ					Wait
	1	4	1	4	1	3 clk
	2	1	1	1	1	0
	3	2	1	2	1	1
		3	1	3	1	2

*1) When the same page access continues:
*2) Signal output from the core
*3) Operates as CAS in interleave mode
*4) Connects to $\overline{CE}$.
*5) Connects to $\overline{OE}$
*6) Can also handle the $\overline{UB}$ and $\overline{LB}$ pins (16-bit bus memory)
*7) Mode change enable: mode where the $\overline{RFSH}$ signals only are output or mode where both $\overline{RFSH}$ and $\overline{OE}$ signals are output.
*8) Valid when additional waits externally inserted are longer than internally inserted waits.

11. 8-BIT TIMERS

The TMP97C241 features eight built-in 8-bit timers (timers 0-7).

Each timer can be operated independently. By cascade-connecting two 8-bit timers, a 16-bit timer can be configured. A pair of 8-bit timers have the following four operating modes:

- 8-bit interval timer mode (x 2)
- 16-bit interval timer mode (x 1)
- 8-bit programmable square wave
  (PPG : variable duty with variable cycle) output mode (x 1)
- 8-bit PWM
  (Pulse Width Modulation: Variable duty with constant cycle) output mode (x 1)

12. 16-BIT TIMERS

The TMP97C241 features two built-in other-function 16-bit timer/event counters (timer 0 and 1).

- 16-bit interval timer mode
- 16-bit event counter mode
- 16-bit programmable square wave output (PPG) mode
- Frequency measurement mode
- Pulse width measurement mode
- Time difference measurement mode

A timer event counter consists of the following:

16-bit up-counter
two 16-bit timer registers (one with double buffer structure)
two 16-bit capture registers
two comparators
capture input control
and timer F/F and its control circuit.

13. SERIAL CHANNELS

The TMP97C241 features three built-in serial channels. Channels 0 and 1 feature a built-in Universal Asynchronous Receiver/Transmitter (UART) and serial I/O s for I/O extension (I/O interface mode). Channel 2 is dedicated to the UART.

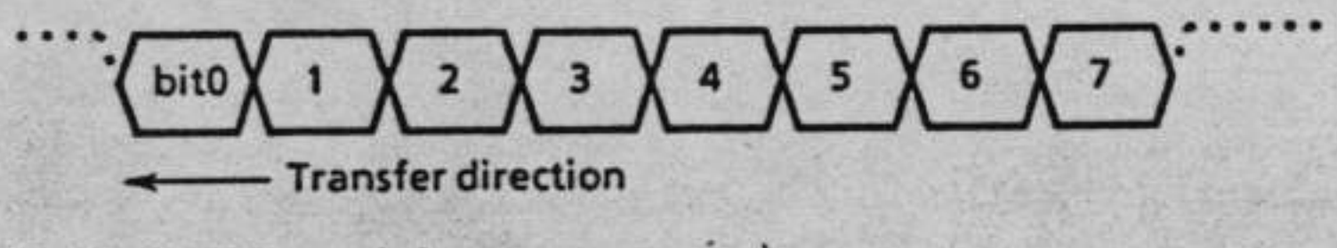
Serial channel operating modes are as follows:

- I/O interface mode (channels 0 and 1) ——— Mode 0 : Used to send/receive I/O data for I/O extension and their synchronous signals (SCLK).
- Universal asynchronous Receiver/Transmitter (UART) mode (channels 0, 1, and 2)
  - Mode 1 : 7-bit send/receive data
  - Mode 2 : 8-bit send/receive data
  - Mode 3 : 9-bit send/receive data

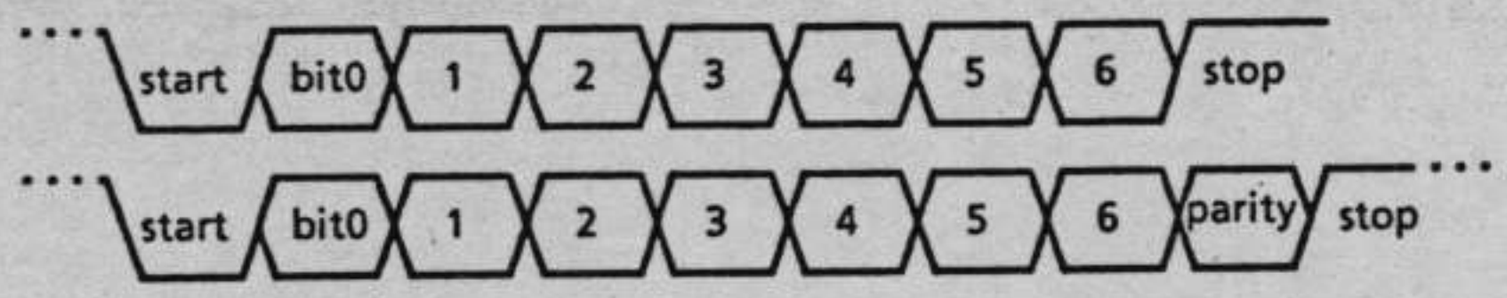
In modes 1 and 2, a parity bit can be added. In mode 3, a wake-up function used by the master controller to start the slave controllers (multi controller system) is provided.

Data formats (for one frame) in each mode are shown below:

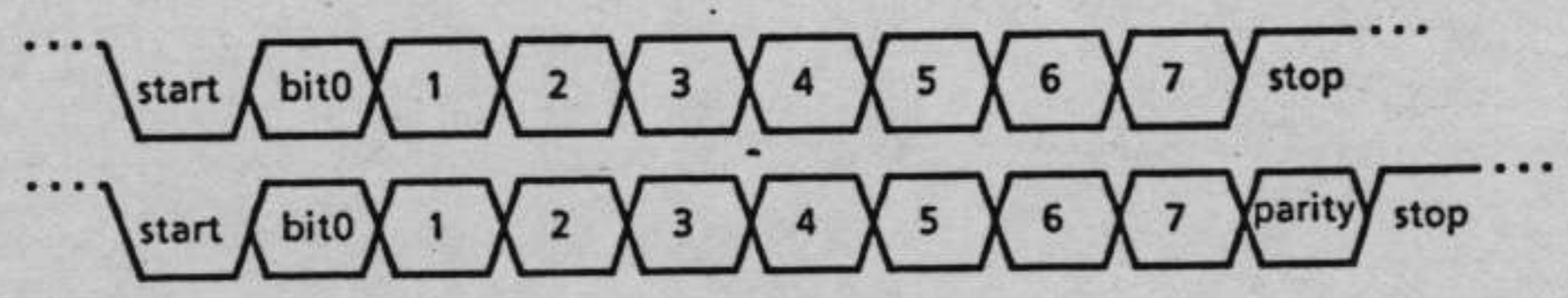
- Mode 0 (I/O interface mode)



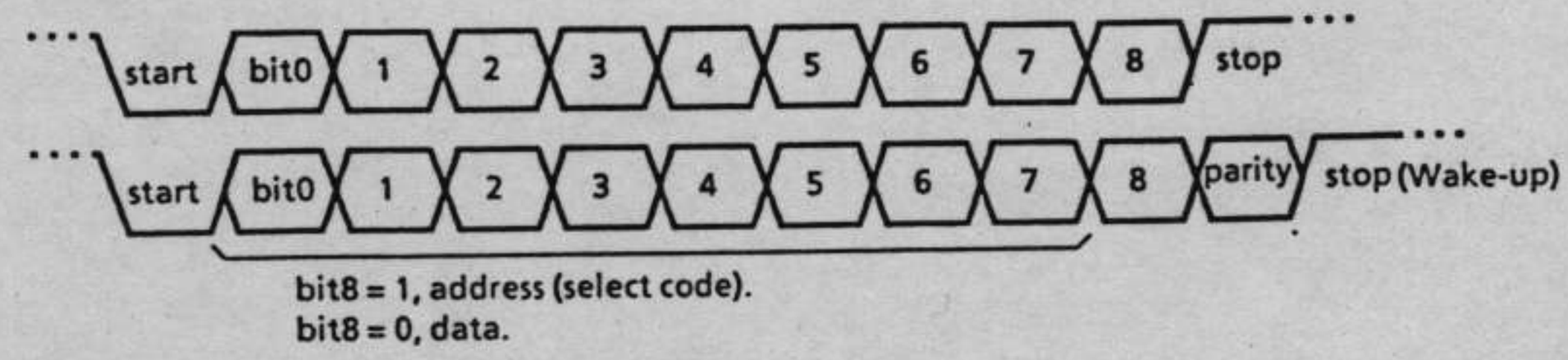
- Mode 1 (7-bit UART mode)



- Mode 2 (8-bit UART mode)



- Mode 3 (9-bit UART mode)



Data formats

14. ANALOG/DIGITAL CONVERTER

The TMP97C241 features a built-in, high-speed, and high-precision 10-bit A/D converter with successive approximation.

Analog input pins (AN7-AN0) for eight channels are also used as an input dedicated port, PF.

15. WATCHDOG TIMER (Runaway Detection Timer)

The TMP97C241 features a built-in watchdog timer (WDT) for detecting runaways. The WDT is used to detect misoperation (runaway) of the CPU caused by, for example, noise, and to return the CPU to normal state. When the WDT detects runaway, it generates a non-maskable interrupt to notify the CPU of the runaway and externally outputs 0 to watchdog timer out pin WDTOUT to notify the peripheral devices.

Connecting the watchdog timer output to the reset pin (in the chip) forces a reset.

16. ELECTRICAL CHARACTERISTICS

Maximum ratings (TMP97C241) (Provisional)

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply voltage	−0.5~6.5	V
V_{IN}	Input voltage	−0.5~Vcc + 0.5	V
Z_{IOL}	Output current (total)	100	mA
Z_{IOH}	Output current (total)	−100	mA
P_D	Power dissipation (Ta = 85°C)	500	mW
T_{SOLDER}	Soldering temperature (10s)	260	℃
T_{STG}	Storage temperature	−65 ~150	℃
T_{OPR}	Operating temperature	−40 ~ 85	℃

DC characteristics (TMP97C241)

(Typical values are for Ta 25oC and Vcc = 5V.)

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL}	Input Low Voltage (P0 - 15)	−0.3	0.8	V	
V_{IL1}	P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC	−0.3	0.3Vcc	V	
V_{IL2}	$\overline{RESET}$, $\overline{NMI}$, INT0~3 (P70~73), $\overline{PS}$	−0.3	0.25Vcc	V	
V_{IL3}	$\overline{EA}$, MODE0, MODE1, XTAL / $\overline{EXCK}$	−0.3	0.3	V	
V_{IL4}	X1	−0.3	0.2Vcc	V	
V_{IH}	Input High Voltage (D0 - 15)	2.2	Vcc + 0.3	V	
V_{IH1}	P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC	0.7Vcc	Vcc + 0.3	V	
V_{IH2}	$\overline{RESET}$, $\overline{NMI}$, INT0~3 (P70~73), $\overline{PS}$	0.75Vcc	Vcc + 0.3	V	
V_{IH3}	$\overline{EA}$, MODE0, MODE1, XTAL / $\overline{EXCK}$	Vcc − 0.3	Vcc + 0.3	V	
V_{IH4}	X1	0.8Vcc	Vcc + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75Vcc 0.9Vcc		V V V	I_{OH} = −400μA I_{OH} = −100μA I_{OH} = −20μA
I_{DAR}	Darlington Drive Current (8 Output pins max.)	−1.0	−3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1 kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ Vcc
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ Vcc − 0.2
I_{CC}	Operating Current (RUN) IDEL1, IDEL2 STOP (Ta = −40~85°C) STOP (Ta = −40~85°C)	TBD TBD TBD	TBD TBD TBD TBD	mA mA μA μA	tosc = 20MHz 0.2 ≤ Vin ≤ Vcc − 0.2 0.2 ≤ Vin ≤ Vcc − 0.2
V_{STOP}	Power Down Voltage (@STOP, RAM Back up)	2.0	6.0	V	V_{IL2} = 0.2Vcc, V_{IH2} = 0.8Vcc
R_1 (Pull up Register)	$\overline{RESET}$, T_{XD}0~2 (P80, P83, P86)	50	150	KΩ	
CIO	Pin Capacitance		10	pF	tosc = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0~3 (P70~73), $\overline{PS}$	0.4	1.0 (Typ)	V	
R_2 (Pull up/down Register)	P5, P6 (P50 Pull down Register)	5	10	KΩ	

Note : I-DAR is guaranteed for a total of up to any 8 output ports among Vcc pins.